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VECTOR COMPILER AND ITS ALGORITHMS

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Abstract

This paper describes the compiling algorithms and techniques for the Hitachi S-810 vector processor. The data dependency analysis method presented here is based on the algorithm by R. Takanuki,et.al.[1] The results are similar to but the approach different from the loop distribution algorithm by D. Kuck, et.al[6]. A new data flow algorithm for data dependency of variables under IF statements is described. For this purpose data flow operators are newly introduced. Some program transformation techniques are shown to be useful for enhancing vectorization. The issues on vector object optimization techniques are also described. With these algorithms, typical vectorization ratio of the S-810 vector compiler is about 30% higher than that of Hitachi's previous vector compiler and more than 680MFLOPS are attained for a FORTRAN program. Most of these algorithms and techniques are easily adaptable to other vector processors.

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Introduction

Over the past decade Hitachi has been developing two types of vector processors and their compilers. One, called IAP(Integrated Array Processor), is integrated in general purpose mainframes. Examples are the Hitachi M180 IAP, M200H IAP, and M280H IAP. Other companies in Japan also make this kind of vector processor, for example, Nippon Electric Company(ACOS1000 IAP) and Mitsubishi(MELCOM COSMO700 IAP). The conceptual base of IAP is transparency and high cost/performance. Transparency is achieved through the interruptable vector instructions(thus they are memory-to-memory instructions) and automatic vector compilers. Therefore, IAP can be used not only for FORTRAN programs in batch mode but also for APL programs in interactive mode. The IAP system can be put together with a small amount of extra hardware. However, the performance ratio of IAP to scalar processor is generally not so high. A typical performance ratio for IAP is about 2 to 3 , with a maximum ratio of about 10.

The other type of vector processor is the Hitachi S-810 model 20 and model 10. This type is a dedicated scientific super computer with vector registers. Other companies in Japan have developed or have been developing this type as well, e.g., Fujitsu(VP-200 and VP-100), and Nippon Electric Company(SX-2 and SX-1). The primary goal of these processors is high performance. But user friendliness is also important, and the automatic vector compiler is the key to achieving this goal.

A basic data dependency algorithm has been developed for the M18Ø and M2ØØH IAP compiler[1]. Techniques for vectorizing IF statements and program transformation techniques have been developed for the M28ØH IAP compiler[4],[5],[12]. Based on the above algorithm and techniques, we have developed extended vectorization techniques and algorithms for the S-81Ø compiler to enhance vectorization and to generate more efficient vector objects.

In this paper, we first briefly describe basic algorithms for data dependency analysis. The data dependency analysis under IF statements is then explained. Finally, the issues on vector object optimization are described.

Data Dependency Analysis

To vectorize FORTRAN programs automatically, the order of operation execution in DO loops has to be changed. In the scalar processing mode, one operation is executed for each index value. After all operations in a DO loop are executed for an index value, the index value is incremented, and each operation is executed again for the new index value, and so on. In the vector processing mode, each operation is executed for all index values, and the next operation is executed for all index values, and so on. This change in execution order is called loop distribution or vectorization (Fig-1).

```
  FORTRAN DO loop          Vector mode

     DO 1Ø i=1,N
     A(i)=B(i)+C(i)   =>  (A_i=B_i+C_i,i=1,N)
  1Ø D(i)=A(i)*E(i)       (D_i=A_i*E_i,i=1,N)
```

Fig. 1 Loop Distribution(Vectorization)

Whether or not a loop distribution is permissible depends on the value defined and its usage for each data. This dependency is generally called data dependency. Data dependency analysis has been studied for many years for variables in the field of scalar object optimization. However, the study of data dependency analysis of arrays for vectorization is relatively new. One study publicized in this field is the work done by D. Kuck,et.al.[6].

The method of data dependency analysis described here is slightly different from theirs. In this method, data dependency relations are classified into five categories: the first is suitably dependent, the second unsuitably dependent, the third specially dependent, the fourth unknown dependent, and the fifth independent.

Examples of the unsuitably dependent case are shown in Fig. 2. Array A is unsuitably dependent in DO 1Ø, whereas variables S is unsuitably dependent in DO 2Ø.

```
   DO 1Ø i=1,N
   A(i-1)=B(i)+C(i)
1Ø D(i)=A(i)*B(i)

   DO 2Ø i=1,N
   A(i)=S*B(i)
2Ø S=C(i)+A(i)
```

Fig. 2 Unsuitably Dependent Case

The <u>specially dependent case</u> is a variation of unsuitably dependent case. Examples of the specially dependent case are shown in Table 1. These special operations can be vectorized with special hardware support.

Table 1 Specially Dependent case

Macro Operation	Example
Vector Sum	S=S+A(i)
Vector Product	S=S*A(i)
Inner Product	S=S+A(i)*B(i)
Vector Iteration	A(i+1)=A(i)*B(i)+C(i)
Vector Max	S=MAX(S,A(i))
Vector Min	S=MIN(S,A(i))

This basic dependency analysis is done for variables and for arrays according to the following two rules:

(1) A variable is <u>unsuitably</u> <u>dependent</u> if there is a defining occurrence and its first occurrence is not a defining occurrence.

(2) An array is <u>unsuitably</u> <u>dependent</u> if one of the two occurrences is a defining occurrence and the preceding occurrence contains a subscript, the value of which is "less than"(*) the value of the subscript of the succeeding occurrence.

For more details on the basic algorithm, see[1].

(*) The value of subscript F_i is "less than" the value of subscript F_j

iff

$$p,q(1\leq p<q\leq n)\ f_iq=f_jp$$

where $F_i=(f_i1,f_i2,\ldots\ldots,f_in)$ and

$$F_j=(f_j1,f_j2,\ldots\ldots,f_jn)$$

are ordered set of subscript values.

The vectorization analysis is based on this basic algorithm[1] and is enhanced by the program transformation techniques. At least three program transformation techniques are related to data dependency analysis. These are <u>statement exchanging</u>, <u>loop</u> <u>splitting</u>, and <u>loop</u> <u>unrolling</u> for a cyclic index.

During data dependency analysis if two statements are exchangeable, they are exchanged to reduce unsuitable dependency. Two statements are <u>exchangeable</u> iff variables/arrays in two statements are mutually unsuitably dependent or independent but not suitably dependent nor unknown.

In the course of the data dependency analysis, a loop is split into vectorizable parts and unvectorizable parts. The <u>loop splitting</u> algorithm is as follows:

(1) Let an assignment statement or a conditional statement be a <u>S-Block</u>(Split-Block).

(2) Analyze data dependencies within a vectorizable S-Block and among S-Blocks and mark unvectorizable on the S-Block if it contains unsuitably dependent or unknown dependent variables/arrays.

(3) Combine adjacent unvectorizable S-Blocks. Repeat step 2 until all S-Blocks are checked.

(4) Combine adjacent vectorizable S-Blocks.

The resultant S-Block is quite similar to the PI-Block produced by the data dependency graph[6].

Data dependency analysis is effective only for linear indexes. Data dependency analysis for non-linear indexes, such as indirect addressing is quite difficult. Therefore, an array with a non-linear index can be vectorized if its occurrences are use only or it appears only once. Otherwise it should be declared independent by the user. (Fig. 3)

```
*VOPTION VEC
      DO 1Ø i=1,N
      A(L(i))=A(L(i))+B(i)
   1Ø CONTINUE
```

Fig. 3 Forced to Vectorize Case

A cyclic index is a non-linear index. A program with a cyclic index, however, can be vectorized through a <u>loop unrolling</u> technique. In Fig. 4 cyclic index j is removed by loop unrolling.

```
   Original loop          Unrolled loop

    j=N                   A(1)=B(N)+C(1)
    DO 1Ø i=1,N           DO 1Ø i=2,N
    A(i)=B(j)+C(i)   =>   A(i)=B(i-1)+C(i)
 1Ø j=i                1Ø CONTINUE
```

Fig. 4 Loop Unrolling for Cyclic Index

<u>Vectorizing IF Statements</u>

To vectorize IF statements, control flow and data flow, or data dependency under IF statements are first analyzed.

The main purposes of control flow analysis are to detect anomalies, such as internal loops, or branches into control structures (see Fig. 5) and clarify control and controlled relationships.

```
    DO 1Ø i=1,N
    IF(e1) GOTO 2
  1     s1
     GOTO 3
  2  IF(e2) THEN
          s2
      ELSE
          s3
          GOTO 1
      END IF
  3  s4
 1Ø CONTINUE
```

Fig. 5 An Anomalous Control Structure

Control flow analysis is relatively easy and little is new to vector compilers.

The situation is different for data flow analysis. Data dependency of arrays within IF statements is the same as that without IF statements. However data dependency of variables with IF statements is slightly different.(Fig. 6)

```
Case A:  IF(  ) THEN
           S=...
         ELSE
           ..=S
         ENDIF
          ...=S

Case B:  IF(  ) THEN
           S=...
         ELSE
           S=...
         ENDIF
          ...=S

Case C:  IF(  ) THEN
           S=...
           ..=S
         ELSE
           ...
         ENDIF
```

Fig. 6 Data Dependency Under IF

Case A is unvectorizable, even though the definition of variable S precedes its use textually. Case B is vectorizable, since the variable is totally defined and both definitions precede its use. Case C is vectorizable, though the variable is partially defined.

The data dependency condition is modified as follows:

(1)′ A variable is <u>unsuitably</u> <u>dependent</u> if there is a defining occurrence and there is a path on which the defining occurrence does not precede the other occurrence.

To check the above condition, the <u>depth-first</u> traverse approach are first attempted for the IAP compiler. This method is simple and there is no extra memory except for backtracking. However it was too slow to analyze a fairly large DO loop with many IF statements. Therefore we have introduced <u>if-then-else</u> <u>reduction</u> <u>method</u> which reduces if-then or if-then-else branches and that makes the depth-first method practical.[12] Nevertheless, the depth-first method is intrinsically time consuming process.

So we have developed the <u>breadth-first</u> data flow method for the S-81Ø compiler. To facilitate this method we have introduced the data flow operators, $\cap^*$ and U*.

For each variable v and each index i in flow graph, there are three data flow variables $IN_i(v)$, $OWN_i(v)$, $OUT_i(v)$ defined as follows:

$$IN_i(v) = \bigcap^*_{j \in Pred(i)} OUT_j(v)$$

$$OWN_i(v) = \begin{cases} -1 & \text{(use precedes)} \\ \emptyset & \text{(not appear)} \\ 1 & \text{(def precedes)} \end{cases}$$

$$OUT_i(v) = IN_i \ U^* \ OWN_i(v)$$

Here, $IN_i(v)$ is the input status for the variable v in vertex i, $OWN_i(v)$ is the own status for the variable v in vertex i, $OUT_i(v)$ is the output status for the variable v in vertex i.

Semantics of $\cap^*$ and U* is defined in Table 2.

Table 2. Data flow operators.

$\cap^*$

	-1	Ø	+1
-1	-1	-1	-1
Ø	-1	Ø	Ø
+1	-1	Ø	+1

U*

		OWN		
		-1	Ø	+1
IN	-1	-1	-1	-1
	Ø	-1	Ø	+1
	+1	+1	+1	+1

Unary $\cap^*$ is defined by binary $\cap^*$ as follows:

$\cap^*Xj$ = X1 $\cap^*$X2 $\cap^*$ .... $\cap^*$Xn
j=1..n

Using these operators and status variables, the flow graph is traversed in breadth-first order. If the value OUT of the final vertex is not -1, then it is suitably dependent. (See the example in Fig. 7)

This algorithm is efficient in the sense that each vertex is traversed only once. In general this algorithm is quite useful for various data dependency of variables, such as variables under nested IF statements or partially defined variables.

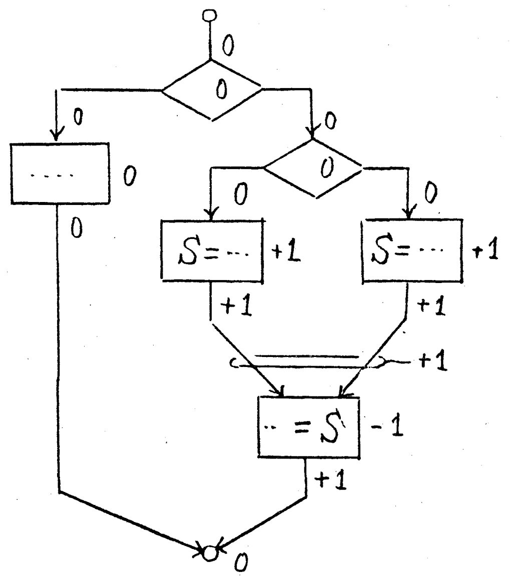

Fig. 7 Example of Data Flow Analysis

Vectorization of IF statements be extended based on the algorithm. For example, if semantics analysis is employed, some special cases can be vectorized as well. Such an example is shown in Fig. 8.

```
      DO 10 i=1,N
      IF(A(K).EQ.X) S=B(I)
      C(I)=S*D(I)
   10 CONTINUE
```

Fig. 8 Semantics analysis of IF statement

This example is an unsuitably dependent case by definition, since there is a definition of a variable and there is a path on which there is no preceding definition of the usage. However, when the semantics of IF statement is considered, this IF expression is index independent(we call this type of IF statement loop invariant IF statement). Therefore this definition of the variable is either always executed or not executed at all for all index values. Thus this type of variables can be vectorized.

The other technique for enhancing vectorization of IF statement is related to the program transformation techniques. One example is the loop unrolling of edge conditions. (See Fig. 9) IF statement of edge condition is removed by loop unrolling.

```
    DO 1Ø i=1,N
    IF(i.EQ.1) THEN         A(1)=Ø.Ø
     A(i)=Ø.Ø               DO 1Ø i=2,N
    ELSE             =>      A(i)=S*B(i)
     A(i)=S*B(i)         1Ø CONTINUE
    END IF
 1Ø CONTINUE
```

Fig. 9 Loop Unrolling for Edge Condition

Vector Object Optimizations

Object optimization techniques for vector compilers are vector text optimizations, vector register assignments, vector memory managements, and other machine dependent optimizations.

Vector text optimization is a common technique for the IAP and the S-81Ø vector processor and it is similar to scalar text optimization. Some of the vector text optimization techniques are common expression elimination, invariant expression moveout, and dead code elimination. Among them the first two are most effective for vector processors.

Vector register assignment is the one of the important tasks for the S-81Ø type vector processor. Vector memory management is the important task for IAP type vector processors. Main target of vector memory management is the efficient use of temporary vector in memory.

Examples of machine dependent optimization for the S-81Ø are:

(1) Use of VMA(Vector Multiply and Add) instruction instead of VM(Vector Multiply) and VA(Vector Add).

(2) Parallel execution of vector instructions with their preparing instructions.(Fig. 1Ø)

```
   DO 1Ø j=1,N
   A(1,j)=Ø.Ø
     DO 1Ø i=2,N
1Ø   A(i,j)=B(i,j)+C(i,j)
```

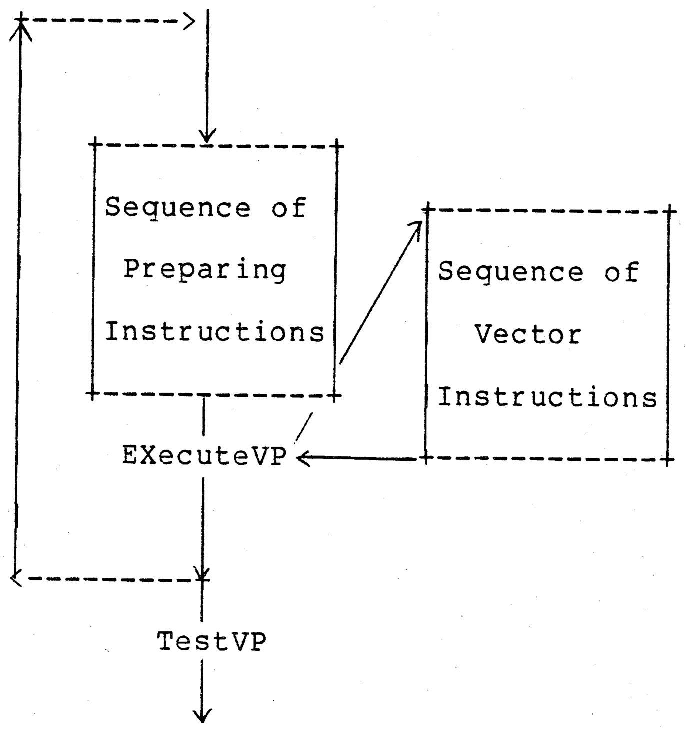
Sequence of Preparing Instructions
Sequence of Vector Instructions
EXecuteVP
TestVP

Fig. 1Ø Scalar/vector Parallel Execution

(3) Compression of vector arguments for intrinsic functions under IF statements.(Fig. 11)

```
      DO 1Ø i=1,N
      IF(A(i).NE.Ø) THEN
        B(i)=SQRT(A(i))
      ENDIF
   1Ø CONTINUE
```

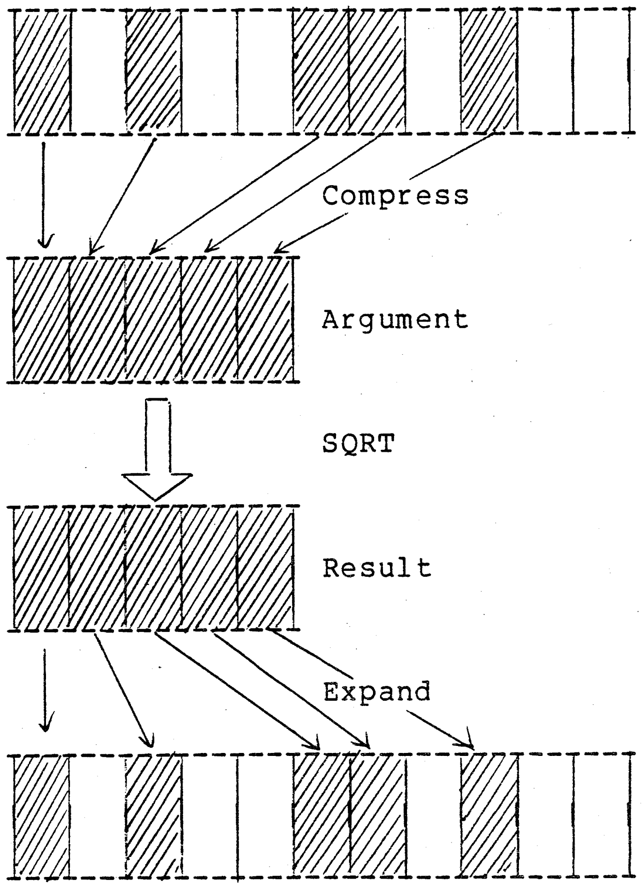

Fig. 11 Compression of Function Argument

Among these optimization techniques, the vector register assignment is the most important and most difficult one. Little has been reported on vector register assignment. The strategy should be different from scalar register assignment, since vector processors like S-810 execute multiple vector instructions in parallel and the access to the same vector register by different instructions may hinder their parallel execution. The vector instruction specification also imposes some restrictions on the vector register assignment for each instruction. Thus we employ tabulated LRU (Least Recently Used) method to assign vector registers in place of simple Round-Robin.

Conclusion

Though the basic data dependency analysis of S-810 is the same as that of IAP, a lot of techniques of enhancing vectorization are used for the S-810 compilers. Some are shown in this paper, but some are not. With these enhancement, the vectorization ratio of typical FORTRAN programs has increased about 30%. And the performance ratio of S-810 vector mode to scalar mode is about 10-100. Maximum speed which was attained for a thermal conduction program written in FORTRAN program compiled by the S-810 compiler is 687 MFLOPS(Million Floating Operations Per Second).

Thus the algorithms and techniques developed for the S-810 vector compiler are effective as well as practical. Some program transformation techniques are especially useful for enhancing vectorization. We believe that program transformations by vector compilers should be further extended to vectorize much more ordinary programs.

References

[1] R. Takanuki, Y. Umetani and I. Nakata, "Some Compiling Algorithms for an Array Processor", Proceedings of 3rd USA-JAPAN Computer Conference, pp 273-279, 1978.

[2] Y. Umetani, S. Kawabe, H. Horikoshi and T. Odaka, "An Analysis on Applicability of the Vector Operations to Scientific Programs and the Determination of an Effective Instruction Repertoire", ibid, pp 331-335,1978.

[3] R. Takanuki and Y. Umetani, "Optimizing FORTRAN77", Hitachi Review, vol. 3Ø,No. 5 ,1981.

[4] Y. Umetani and M. Yasumura, "A Vectorization Algorithm for Control Statements", Journal of Information Processing, To be published.

[5] M. Yasumura, Y. Umetani and H. Horikoshi, "Partial Vectorization Method for Automatic Vector Compilers", Journal of Information Processing(in Japanese), Vol.24, No.1, 1983.

[6] D. Kuck, R. Kuhn, D. Padua, B. Leasure and M. Wolfe, "Dependence Graphs and Compiler Optimizations", Proceedings of the 8th ACM Symposium on Principles of Programming Languages, pp 2Ø7-218, 1981.

[7] D. A. Padua, D. J. Kuck, and D. H. Lawrie, "High-Speed Multiprocessors and Compilation Techniques", IEEE

Transaction on Computer, Vol. C-29, pp 763-776, Sept. 1980.

[8] D. J. Kuck, "Parallel Processing of Ordinary Programs", Advances in Computer, Academic Press, Vol.15, 1976.

[9] A. V. Aho and J. D. Ullman, "Principles of Compiler Design", Addison-Wesley, 1977.

[10] D. B. Loveman, "Program Improvement by Source-to-Source Transformation", Journal of the ACM, Vol. 20, No. 1, Jan. 1977.

[11] R. L. Sites, "An Analysis of the CRAY-1 Computer", Proceedings of the 5th Annual Symposium on Computer Architecture, pp101-106, 1978.

[12] M. Yasumura, T. Matsunaga, Y. Tanaka, and Y. Umetani, "A Method of Control Structure Analysis for a Vector Compiler", Proceedings of National Conference of Information Processing Japan (in Japanese), pp211-212, Oct. 1981.