

Proof Nets and Boolean Circuits

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Motivation (1)

- Proofs-as-Programs (Curry-Howard) correspondence:

Proofs = Programs

Cut-Elimination = Computation

(Normalization)

- Usually interested in **infinite, uniform, sequential** computation such as **functional programs**.
- Can be extended to **finite, nonuniform, parallel** computation such as **boolean circuits**?

Motivation (2)

● Our goal:

Proofs = Circuits

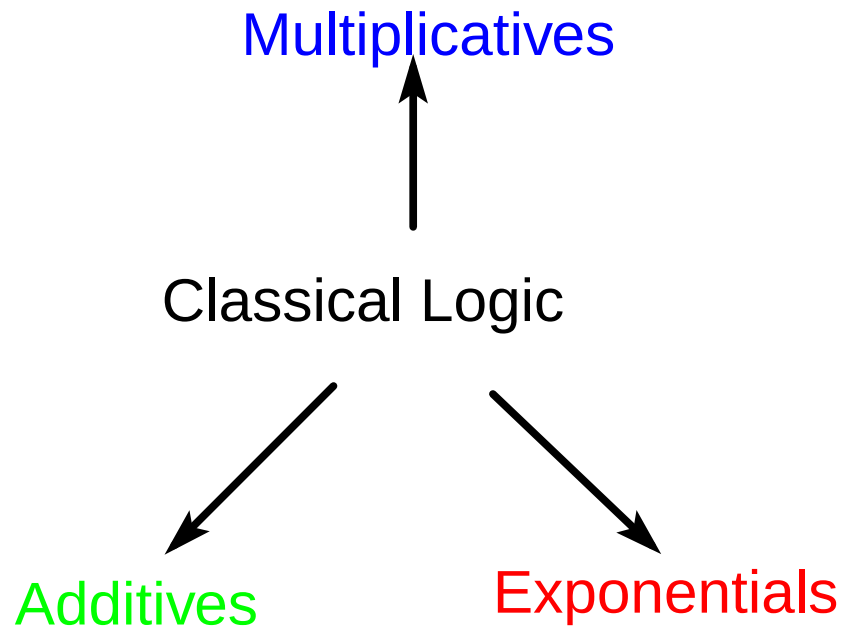
Cut-Elimination = Evaluation

● What system of Proofs?

● Cut-elimination in Classical/Intuitionistic Logics:
Non-elementary time. Too much!

Motivation (3)

- Linear Logic (Girard 87): a decomposition of Classical/Intuitionistic Logics:



- MLL: Classical Logic without weakening nor contraction.
- Has a nice parallel syntax: Proof Nets (Girard 87).
- Quadratic time cut-elimination procedure.

Motivation (4)

- Our specific goal: correspondence between MLL proof nets and circuits.
- (Mairson & Terui 2003) Encoding of circuits by linear size MLL proof nets $\implies$ P-completeness of cut-elimination in MLL.
 - “Proof nets can represent all finite functions as SIZE-efficient as circuits.”
- What about the DEPTH-efficiency? What about the converse?

Parallel computation

- **Effective parallelization:** Achieve a dramatic speed-up by use of a reasonable number of processors.
- Addition: School method ($O(n)$ time)
⇒ Parallel algorithm: (constant time)
- In boolean circuits,

$$\text{time} = \text{depth}$$

$$\text{num of processors} = \text{size (num of gates)}$$

- **Fundamental question:** Are all feasible algorithms effectively parallelizable?
- **$NC = P$ problem:** Are all problems in P solvable by polynomial size poly-log depth circuits?

Outline

- Unbounded fan-in boolean circuits.
- Proof nets for **MLLu** and parallel cut-elimination procedure.
- Simulation of circuits by proof nets
- Simulation of proof nets by circuits
- Proof net complexity classes

Boolean circuits (1)

- An **unbounded fan-in circuit** with n inputs (and 1 output): a directed acyclic graph made of
 - **input nodes** $x_1, \dots, x_n$
 - **boolean gates** $\neg, \wedge, \vee$ (and possibly more).(there is a distinguished node for **output**.)
- $\wedge$ and $\vee$ may have an arbitrary number of inputs.
- **size** = the number of gates
- **depth** = the length of the longest path

Boolean circuits (2)

- A circuit C **accepts** $w = i_1 \cdots i_n \in \{0, 1\}^n$ if $C[x_1 := i_1, \dots, x_n := i_n]$ evaluates to 1.
- C **accepts** $X \subseteq \{0, 1\}^n$ if C accepts $w \Leftrightarrow w \in X$.

Formulas of MLLu

Formulas:

$\alpha, \alpha^\perp$

Literals

$\otimes^n(A_1, \dots, A_n), \quad n \geq 2$ n -ary Conjunction

$\wp^n(A_1, \dots, A_n), \quad n \geq 2$ n -ary Disjunction

Negation: defined by

$$(\otimes^n(A_1, \dots, A_n))^\perp \equiv \wp^n(A_n^\perp, \dots, A_1^\perp)$$

$$(\wp^n(A_1, \dots, A_n))^\perp \equiv \otimes^n(A_n^\perp, \dots, A_1^\perp)$$

Notation:

$$A \otimes B \equiv \otimes^2(A, B) \quad A \wp B \equiv \wp^2(A, B) \quad A \multimap B \equiv A^\perp \wp B$$

Sequent calculus for MLLu

● **Sequents:** $\vdash \Gamma$, where Γ is a multiset of formulas.

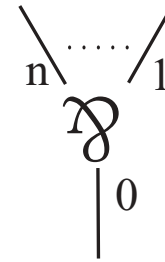
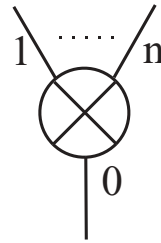
● **Inference Rules:**

$$\frac{}{\vdash A, A^\perp} \text{ (Axiom)} \qquad \frac{\vdash \Gamma, C \quad \vdash \Delta, C^\perp}{\vdash \Gamma, \Delta} \text{ (Cut)}$$
$$\frac{\vdash \Gamma_1, A_1 \quad \dots \quad \vdash \Gamma_n, A_n}{\vdash \Gamma_1, \dots, \Gamma_n, \otimes^n(A_1, \dots, A_n)} \otimes^n \qquad \frac{\vdash \Gamma, A_1, \dots, A_n}{\vdash \Gamma, \wp^n(A_1, \dots, A_n)} \wp^n$$

● Exchange is implicit. No weakening, no contraction.

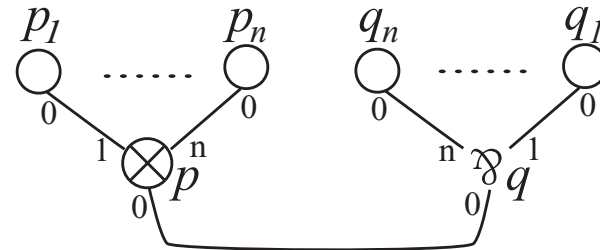
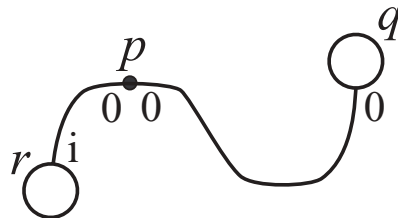
Proof nets for MLLu

Links:



Each link has several **ports**. **Principal port(s)** numbered 0.

Cut: an edge connecting two principal ports.

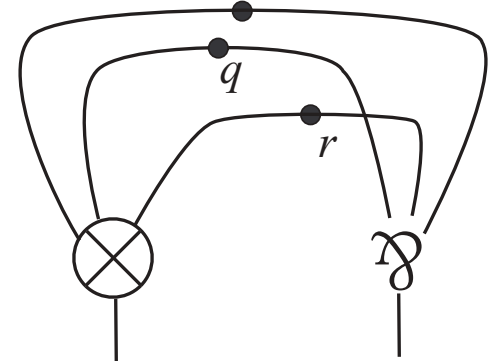


Proof nets are obtained from sequent proofs by extracting their structures (forgetting about formulas).

Example: Negation

$$\frac{
 \frac{
 \overline{\vdash \alpha^\perp \wp \alpha^\perp, \alpha \otimes \alpha} \quad \overline{\vdash \alpha^\perp, \alpha} \quad \overline{\vdash \alpha^\perp, \alpha}
 }{
 \vdash \otimes^3(\alpha^\perp \wp \alpha^\perp, \alpha, \alpha), \alpha^\perp, \alpha^\perp, \alpha \otimes \alpha
 }
 }{
 \vdash \otimes^3(\alpha^\perp \wp \alpha^\perp, \alpha, \alpha), \wp^3(\alpha^\perp, \alpha^\perp, \alpha \otimes \alpha)
 }$$

$\Rightarrow$



Example: Booleans

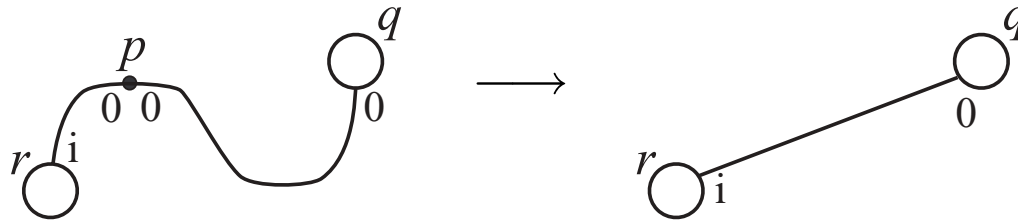
● **B** $\equiv \alpha \multimap \alpha \multimap \alpha \otimes \alpha \equiv \wp^3(\alpha^\perp, \alpha^\perp, \alpha \otimes \alpha)$

$$\frac{\frac{\overline{\vdash \alpha^\perp, \alpha} \quad \overline{\vdash \alpha^\perp, \alpha}}{\vdash \alpha^\perp, \alpha^\perp, \alpha \otimes \alpha} \otimes^2}{\vdash \wp^3(\alpha^\perp, \alpha^\perp, \alpha \otimes \alpha)} \wp^3 \quad \Rightarrow \quad \text{Diagram} \equiv b_1$$

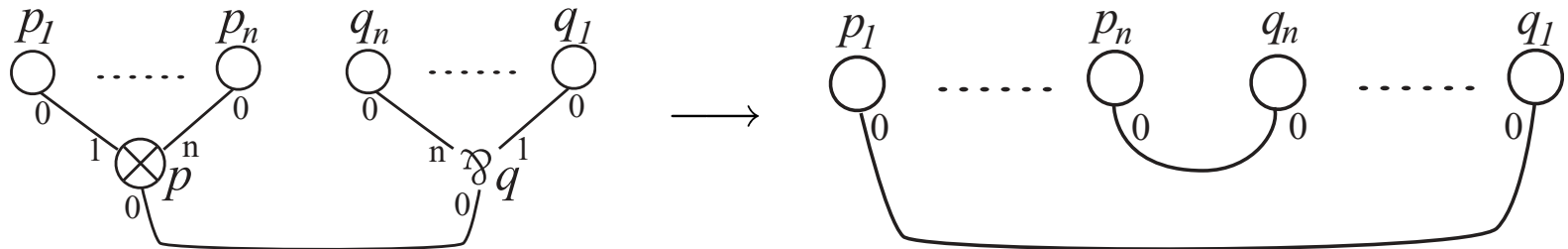
$$\frac{\frac{\overline{\vdash \alpha^\perp, \alpha} \quad \overline{\vdash \alpha^\perp, \alpha}}{\vdash \alpha^\perp, \alpha^\perp, \alpha \otimes \alpha} \otimes^2}{\vdash \wp^3(\alpha^\perp, \alpha^\perp, \alpha \otimes \alpha)} \wp^3 \quad \Rightarrow \quad \text{Diagram} \equiv b_0$$

Reduction rules

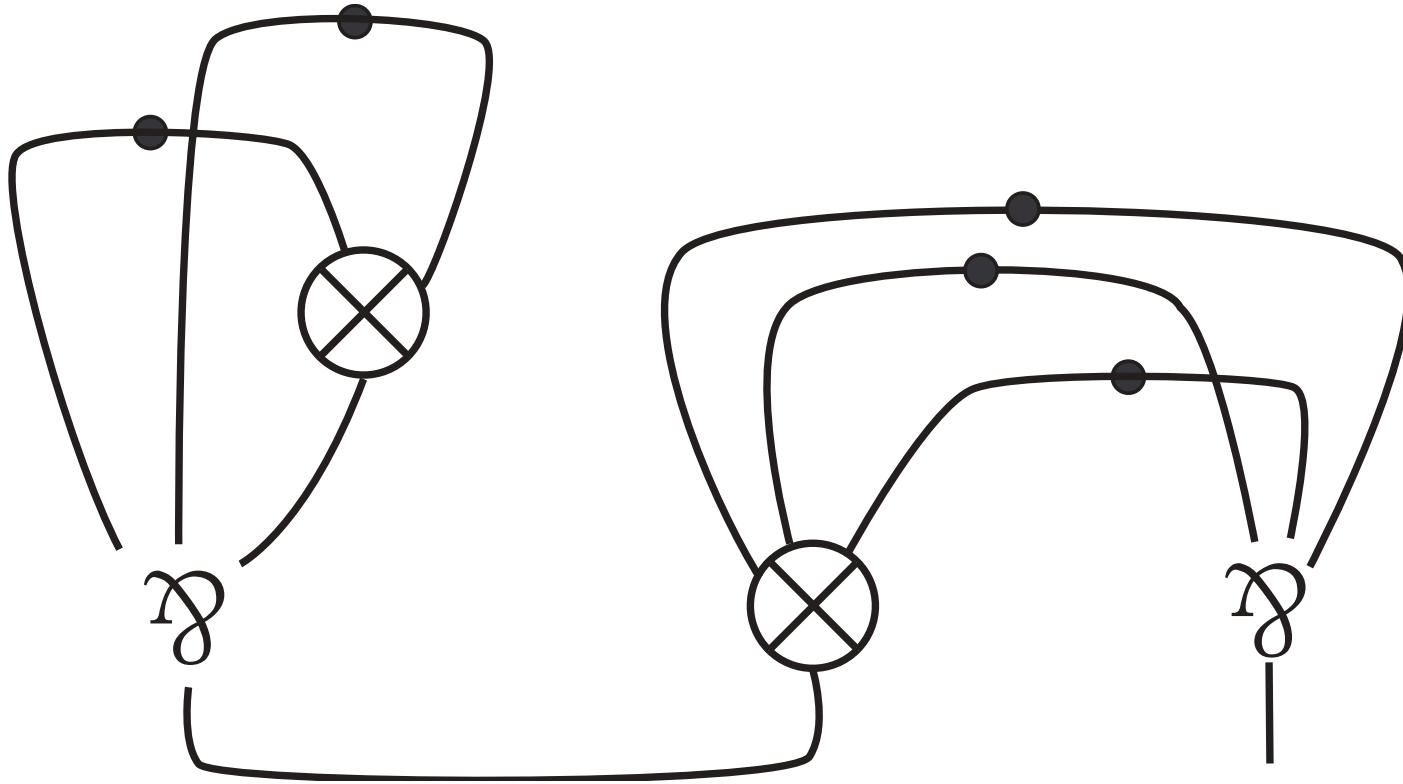
● Axiom reduction:



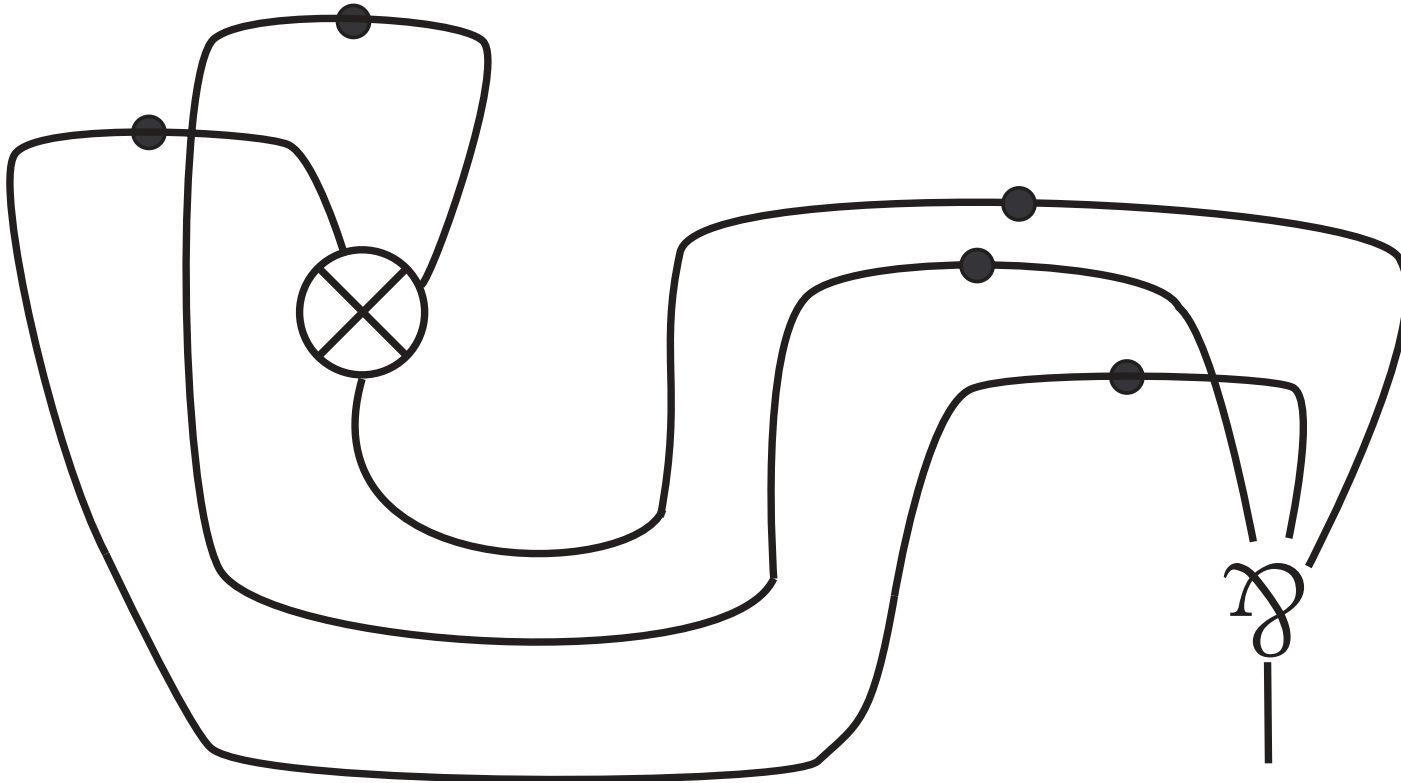
● Multiplicative reduction:



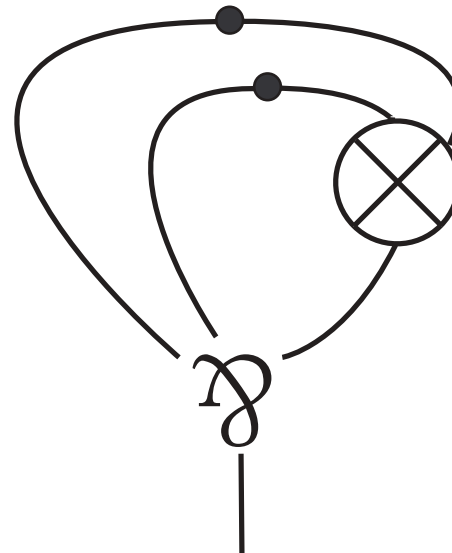
Example: Computing Negation of True



Example: Computing Negation of True



Example: Computing Negation of True



Sequential cut elimination

• Size $|P|$: number of links.

Sequential cut elimination

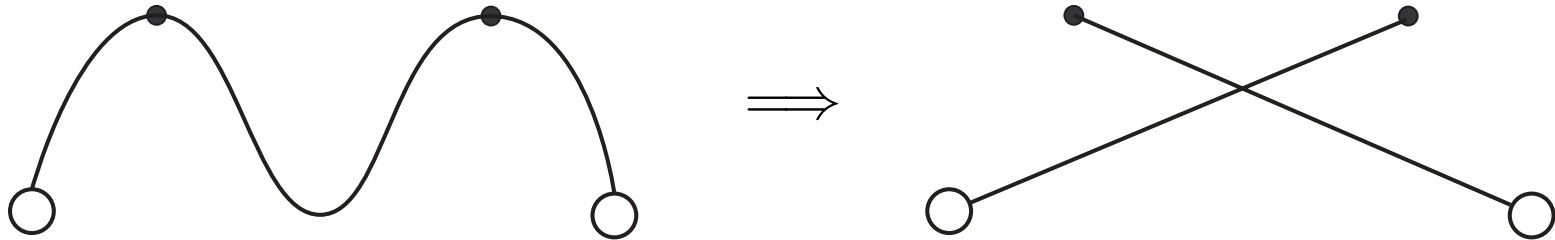
- Size $|P|$: number of links.
- Theorem (Girard 87): Every proof net P reduces to a cut-free proof net in $|P|$ steps.

Sequential cut elimination

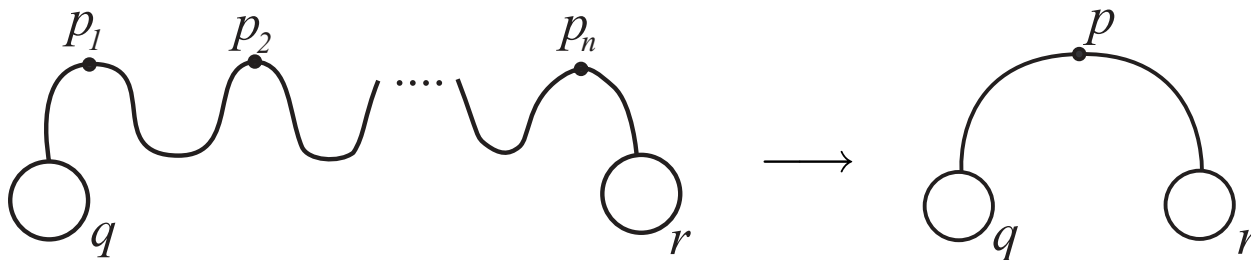
- Size $|P|$: number of links.
- Theorem (Girard 87): Every proof net P reduces to a cut-free proof net in $|P|$ steps.
- Too slow!

Parallel cut elimination (1)

- Applying two axiom reductions in parallel may conflict:

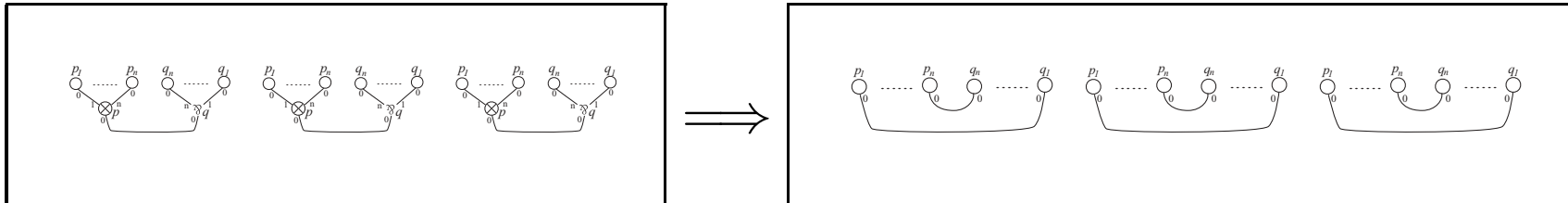


- Global axiom reduction:

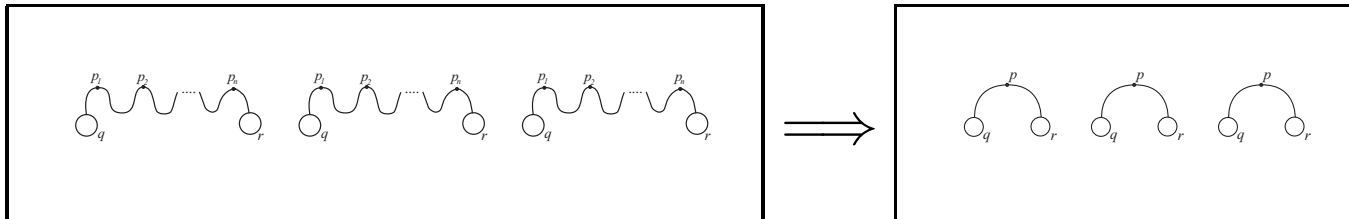


Parallel cut elimination (2)

Parallel multiplicative reduction:



Parallel axiom reduction:



$P_1 \Rightarrow P_2$ if P_2 is obtained from P_1 either by parallel m-reduction or by parallel a-reduction.

Parallel cut elimination (3)

- What controls the runtime of parallel cut-elimination?
- Depth $d(P)$: Maximal depth of cut formulas in it.
(P is assumed to be typed by **principal types** (most general types))
- Depth of formulas:

$$d(\alpha) = d(\alpha^\perp) = 1$$

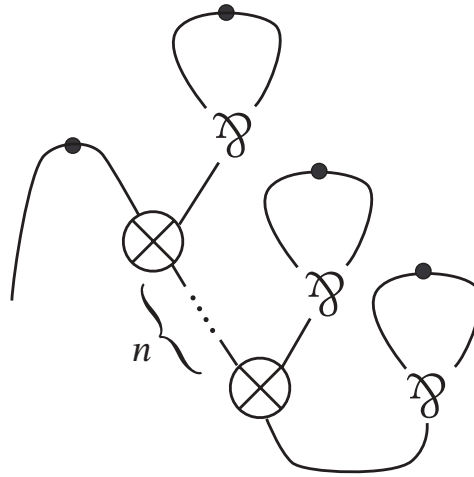
$$\begin{aligned} d(\otimes^n(A_1, \dots, A_n)) &= d(\wp^n(A_1, \dots, A_n)) \\ &= \max(d(A_1), \dots, d(A_n)) + 1 \end{aligned}$$

Parallel cut elimination (4)

- **Theorem:** Every proof net P reduces to a normal form in $2 \cdot d(P)$ parallel reduction steps.
- **Proof:** By applying parallel a-reduction, every cut becomes multiplicative. By applying parallel m-reduction, the depth decreases by 1. □

Limitation on parallelization

● P_n :



- $|P_n|$ and $d(P_n)$ are linear in n .
- Parallel cut-elimination takes almost as long time as sequential cut-elimination.

Representing circuits by proof nets

 Idea: Represent

Circuits by Proof nets

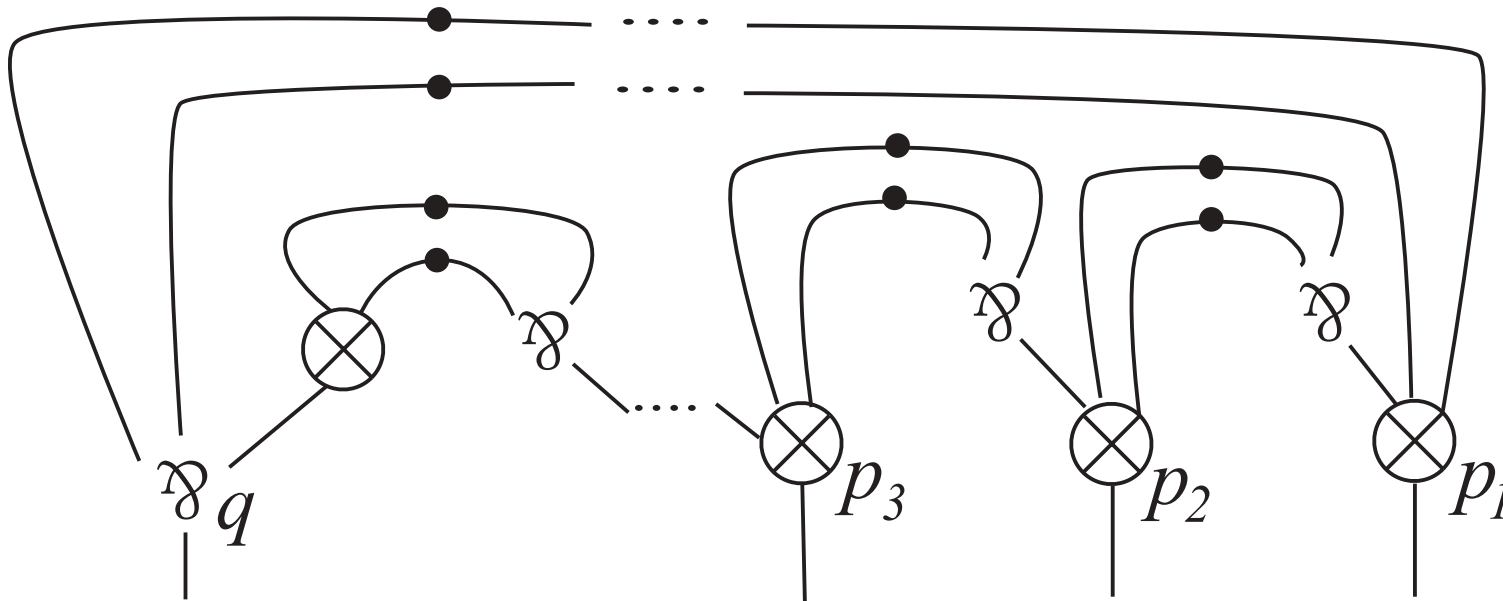
Boolean values by Proof nets (b_1, b_0)

Assignment by Cuts

Evaluation by Cut elimination

Representation of Parity

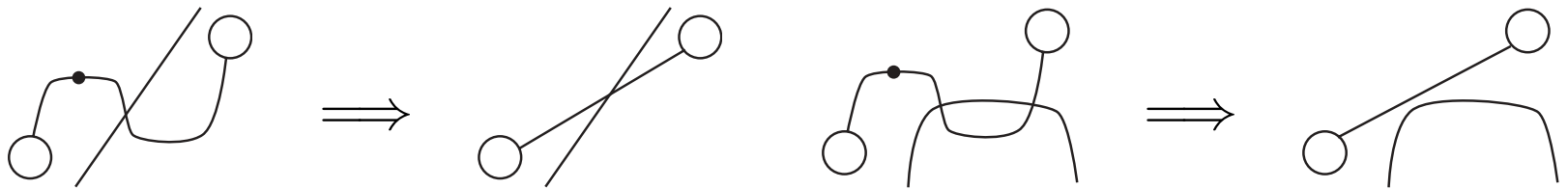
- **Parity**: $\text{PARITY}^n(x_1, \dots, x_n) = 1$ iff the sum of $x_1, \dots, x_n$ is odd.
- **CANNOT** be represented by (poly-size) circuits of constant depth.



- The conclusion is $\vdash \underbrace{\mathbf{B}^\perp, \dots, \mathbf{B}^\perp}_n, \mathbf{B}$
n times

Correctness of parity

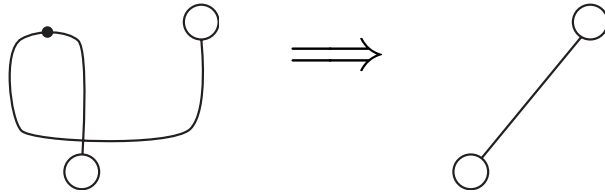
- There are exactly 2 crossings in the drawing.
- Multiplicative reduction does not change the num of crossings.
- Axiom reduction preserves the **parity** of the num of crossings:



- Therefore, the parity is 0 after cut-elimination.

Expressivity of flat proof nets

- Would break down if there were a self-crossing:



- But self-crossing can be avoided.
- As far as proof nets of conclusion $\vdash \underbrace{\mathbf{B}^\perp, \dots, \mathbf{B}^\perp}_{n \text{ times}}, \mathbf{B}$ are concerned, all what matters is the **parity** of the num of crossings.
- Theorem:** Every proof net with the above conclusion represents either PARITY^n or $\neg \text{PARITY}^n$.

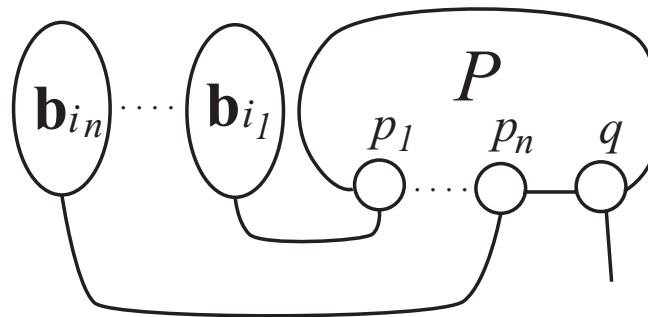
Boolean proof nets

- Boolean proof net: a proof net with conclusion

$$\vdash \mathbf{B}[A_1/\alpha]^\perp, \dots, \mathbf{B}[A_n/\alpha]^\perp, \otimes^m(\mathbf{B}, \vec{G})$$

for some $A_1, \dots, A_n$ and $\vec{G}$ (garbage).

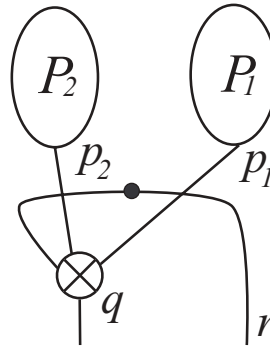
- Given $w = i_1 \cdots i_n \in \{0, 1\}^n$, define $P(w)$ to be:



- P accepts $w \in \{0, 1\}^n$ if $P(w)$ reduces to $\otimes(b_1, \vec{P}_G)$ for some proof nets $\vec{P}_G$ with conclusions $\vec{G}$.

Conditional and Disjunction

• if q then P_1 else P_2



• **Disjunction:** $\text{or}(p, q) \equiv \text{if } p \text{ then } b_1 \text{ else } q$

• Disjunctions of arbitrary arity can be represented by proof nets of constant depth.

Composition:



14/07/04, Turku – p.31/44

Proof Net for Majority (1)

• $\text{MAJ}^n(x_1 \cdots x_n) = 1$ if at least half of x_i 's are 1.

• Let $id, sh : \{0, 1\}^{n+1} \longrightarrow \{0, 1\}^{n+1}$ be:

$$id(i_1 \cdots i_{n+1}) = i_1 \cdots i_{n+1}$$

$$sh(i_1 \cdots i_{n+1}) = i_2 \cdots i_{n+1} i_1$$

• F : higher order functional

$$F(0) = id$$

$$F(1) = sh$$

Proof Net for Majority (2)

• MAJ^n given by

$$\text{MAJ}^n(x_1 \cdots x_n) = \text{FstBit}(F(x_1) \circ \cdots \circ F(x_n) (\underbrace{0 \cdots 0}_{n/2} \underbrace{1 \cdots 1}_{n/2+1}))$$

• Example:

$$\begin{aligned} \text{MAJ}^6(101101) &= \text{FstBit}(F(1)F(0)F(1)F(1)F(0)F(1)(0001111)) \\ &= \text{FstBit}(sh \circ id \circ sh \circ sh \circ id \circ sh(0001111)) \\ &= \text{FstBit}(1110001) \\ &= 1 \end{aligned}$$

• Represented by proof nets of **constant depth**. (**CANNOT** be represented by (poly-size) circuits of constant depth.)

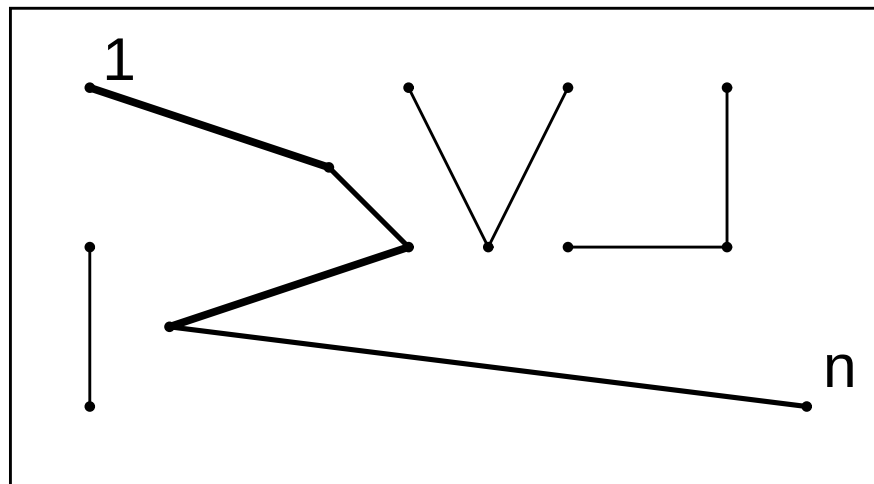
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St-connectivity₂

- **Input:** an undirected graph of degree 2 (i.e., nonbranching graph) with vertices $\{1, \dots, n\}$. Assume it is coded by a $n \times n$ boolean matrix.
- **Output:** is 1 if vertices 1 and n are connected.



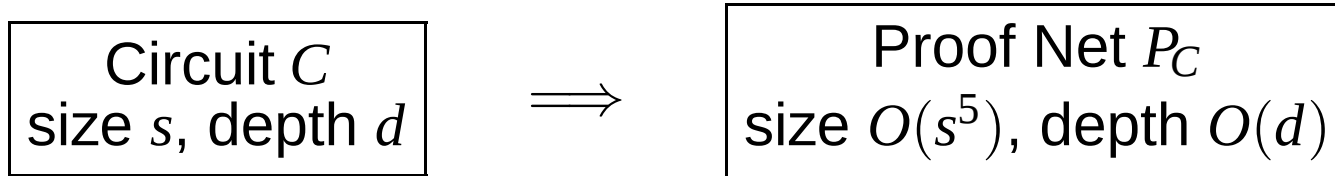
- Can simulate MAJ in constant depth.
- Represented by proof nets of **constant depth**.

From Circuits to Proof nets

- **Theorem:** For every circuit C of size s and depth d (possibly equipped with $stCONN_2$), there is a boolean proof net P_C of size $O(s^5)$ and depth $O(d)$ which accepts the same set as C .

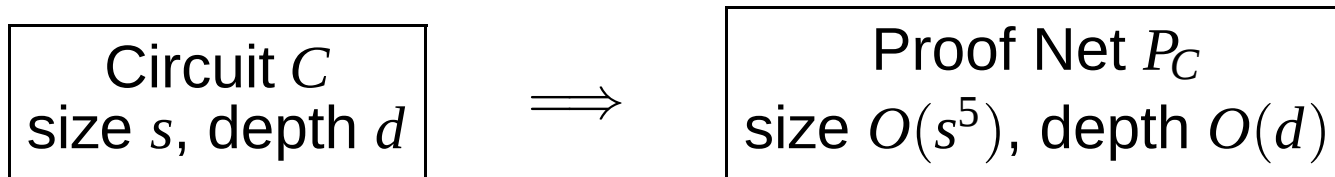
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- **Proof:** $\neg$, $\wedge^n$, $\vee^n$, $stCONN_2^n$ represented by a proof net of size $O(n^4)$ and of constant depth. Composition increases the depth linearly.

Representing proof nets by circuits

🔴 Idea: Represent

A proof net P by a set of boolean values

One-step reduction by constant depth circuit

$2 \cdot d(P)$ reduction steps by $O(d)$ -depth circuit

Coding proof nets by boolean values

• P : a proof net with links $\subseteq L$.

• $Conf(P)$: consists of the following boolean values:

For $p, q \in L$,

$alive(p) \iff p$ is a link of P

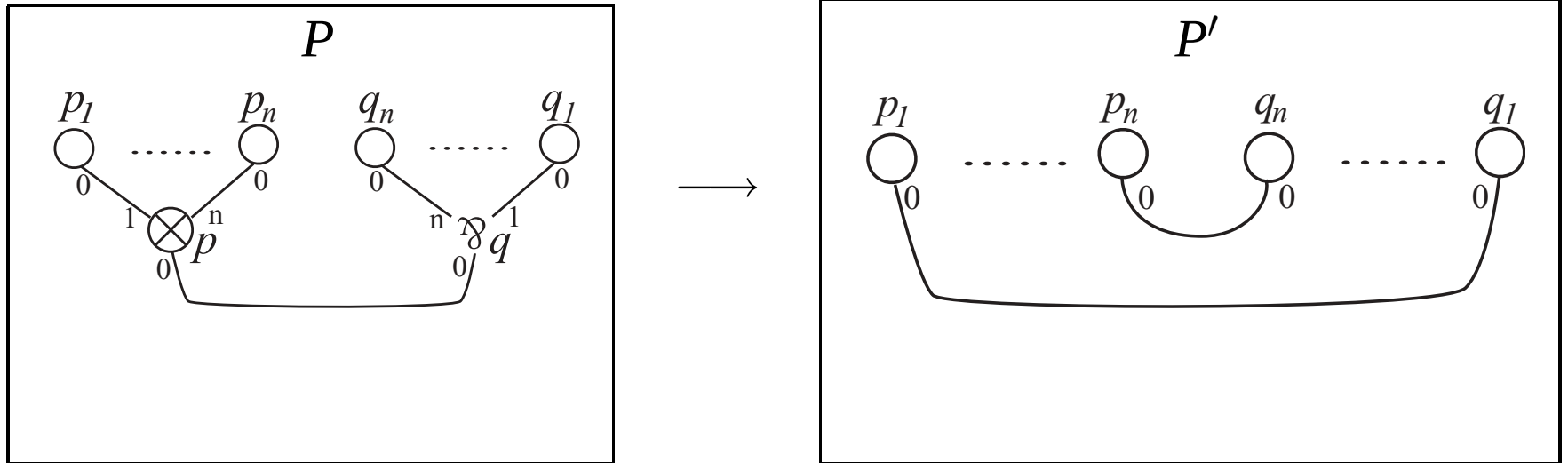
$sort(p, s) \iff$ link p is of sort $s \in \{\otimes, \wp, \bullet\}$

$edge(p, i, q, j) \iff$ there is an edge between port i of link p and port j of link q

• Build a circuit C s.t.

if $P_1 \implies P_2$ then C computes $Conf(P_2)$ from $Conf(P_1)$.

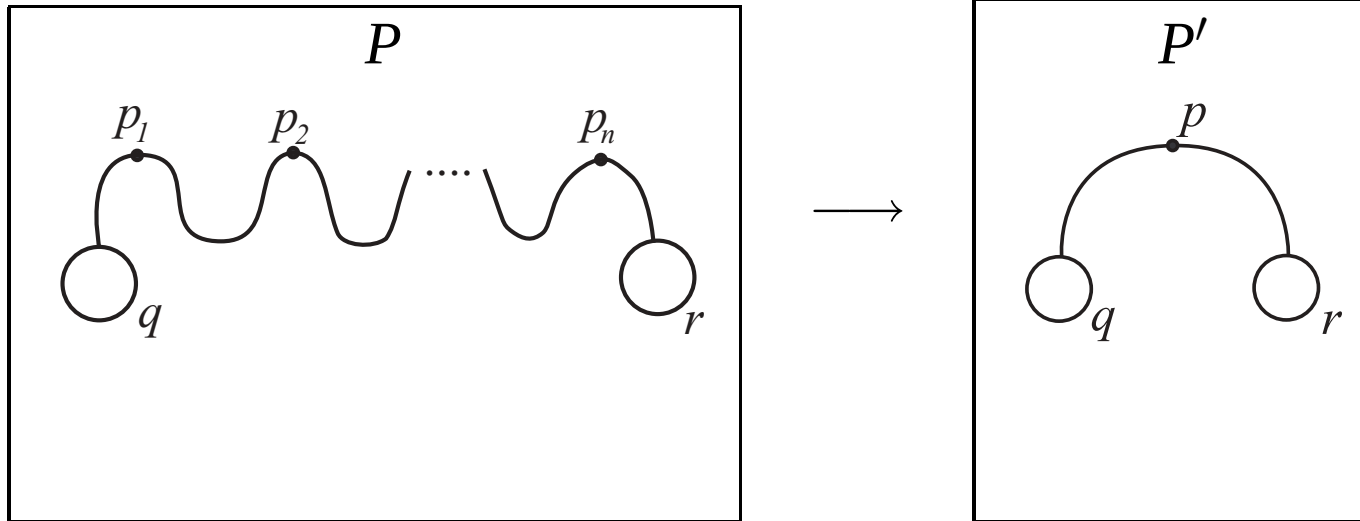
Multiplicative Reduction



➊ Easily implemented by a constant depth circuit: E.g,

$$\begin{aligned}
 \text{edge}'(p_i, 0, q_i, 0) &= \text{edge}(p_i, 0, q_i, 0) \vee \\
 &\quad \bigvee_{p, q \in L} (\text{edge}(p, 0, q, 0) \wedge \bigvee_j \text{edge}(p_i, 0, p, j) \wedge \text{edge}(q_i, 0, q, j))
 \end{aligned}$$

Global Axiom Reduction



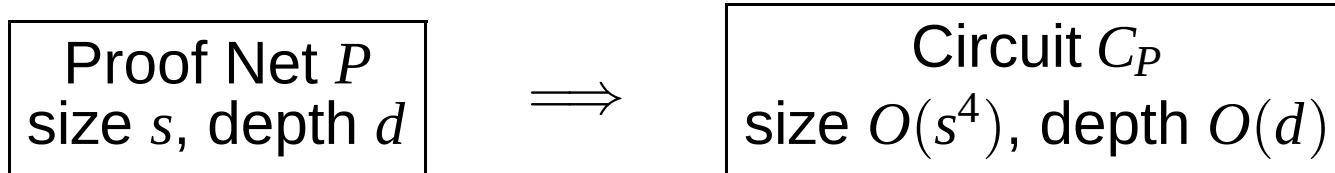
- Naive attempt to build a constant depth circuit leads to exponential size.
- Use $stCONN_2$ gates.
- Apply to the axiom-cut subgraph of P , that is of degree 2.

From Proof nets to Circuits

- **Theorem:** For every boolean proof net P of size s and depth d , there is a circuit C (with $stCONN_2$ gates) of size $O(s^4)$ and depth $O(d)$ which accepts the same set as P .

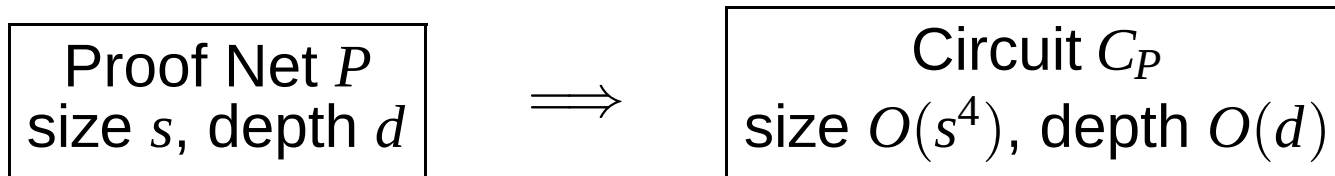
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- **Theorem:** For every boolean proof net P of size s and depth d , there is a circuit C (with $stCONN_2$ gates) of size $O(s^4)$ and depth $O(d)$ which accepts the same set as P .



- **Proof:** Cut-elimination of P requires of $2 \cdot d$ steps. Each step simulated by a constant depth circuit (with $stCONN_2$ gates). Initialization and acceptance checking also by constant depth circuits.

Proof net complexity classes (1)

• For $X \subseteq \{0, 1\}^*$,

$X \in AC^i(\mathcal{F}) \stackrel{def}{\iff} X$ is accepted by a polynomial size $\log^i$ -depth family of unbounded fan-in circuits with additional gates from $\mathcal{F}$.

$X \in APN^i \stackrel{def}{\iff} X$ is accepted by a polynomial size $\log^i$ -depth family of proof nets.

• **Theorem:** For every $i \geq 0$,

$$APN^i = AC^i(stCONN_2).$$

Proof net complexity classes (2)

- $APN = \bigcup_i APN^i$.
- **Theorem** $APN = NC$.
- **Proof:** $AC^i \subseteq AC^i(stCONN_2) = APN^i \subseteq AC^{i+1}$ and $NC = \bigcup_i AC^i$.
- $P/poly$: nonuniform version of P .
- **Theorem** $P/poly$ = the class of languages $X \subseteq \{0,1\}^*$ accepted by polynomial size families of proof nets.
- Note $AC^0(stCONN_2) = L/poly$ (nonuniform logspace). Hence,

$$AC^0 \subsetneq NC^1 \subseteq L/poly = APN^0 \subseteq AC^1$$

Conclusion

- Extended the Proofs-as-Programs paradigm to a finite, nonuniform, parallel setting.
- Characterized proof net complexity by circuit complexity.
- Proof nets represent "higher order gates."

Future Work

- $NC^{i+1} \subseteq APN^i$?
- Comparison with other approaches to proofs-circuits correspondence (Propositional Proof Systems and Bounded Arithmetic).
- Study the bounded fan-in case.
- Implicit parallel complexity.